In the Claims:

Claim 1 (currently amended): A video encoder comprising:

a vertical scaler, wherein said vertical scaler receives a first plurality of video lines at a first frequency and outputs a second plurality of video lines at said first frequency;

a FIFO, wherein said FIFO receives said second plurality of video lines at said first frequency from said vertical scaler, said FIFO outputting said second plurality of video lines at a second frequency such that said second plurality of video lines at said second frequency are horizontally scaled.

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Claim 2 (original): The video encoder of claim 1 wherein said second plurality of video lines are in a first video format.

Claim 3 (original): The video encoder of claim 2 further comprising a modulator/timing generator, wherein said modulator/timing generator receives said second plurality of video lines from said FIFO in said first video format, and said modulator/timing generator converts said first video format into a second video format.

Claim 4 (original): The video encoder of claim 3 wherein said first video format is selected from the group consisting of VGA and SVGA.

Claim 5 (original): The video encoder of claim 3 wherein said second video format is selected from the group consisting of NTSC, PAL, SECAM, and SCART.

Claim 6 (original): The video encoder of claim 3 wherein said first video format is SVGA and said second video format is NTSC.

Claim 7 (original): The video encoder of claim 1 wherein said first frequency is an integer ratio of said second frequency.

Claim 8 (original): The video encoder of claim 1 wherein said first frequency is a non-integer ratio of said second frequency.

Claim 9 (original): The video encoder of claim 1 wherein a first clock has said first frequency and a second clock has said second frequency, and wherein said first clock and said second clock are synchronous.

Claim 10 (original): The video encoder of claim 1 wherein a first clock has said first frequency and a second clock has said second frequency, and wherein said first clock and said second clock are asynchronous.

Claim 11 (currently amended): A method comprising steps of:

receiving by a vertical scaler a first plurality of video lines at a first frequency;

scaling in said vertical scaler said first plurality of video lines at said first frequency into a second plurality of video lines at said first frequency;

outputting by said vertical scaler said second plurality of video lines at said first frequency;

receiving by a FIFO said second plurality of video lines at said first frequency;

outputting by said FIFO said second plurality of video lines at a second frequency such that said second plurality of video lines at said second frequency are horizontally scaled.

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Claim 12 (original): The method of claim 11 further comprising steps of:

receiving by a modulator/timing generator said second plurality of video lines in a first video format;

converting in said modulator/timing generator said second plurality of video lines from said first video format into a second video format.

Claim 13 (original): The method of claim 12 wherein said first video format is selected from the group consisting of VGA and SVGA.

Claim 14 (original): The method of claim 12 wherein said second video format is selected from the group consisting of NTSC, PAL, SECAM, and SCART.

Claim 15 (original): The method of claim 12 wherein said first video format is SVGA and said second video format is NTSC.

Claim 16 (original): The method of claim 11 wherein said first frequency is an integer ratio of said second frequency.

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Claim 17 (original): The method of claim 11 wherein said first frequency is a non-integer ratio of said second frequency.

Claim 18 (original): The method of claim 11 wherein a first clock has said first frequency and a second clock has said second frequency, and wherein said first clock and said second clock are synchronous.

Claim 19 (original): The method of claim 11 wherein a first clock has said first frequency and a second clock has said second frequency, and wherein said first clock and said second clock are asynchronous.

Claim 20 (currently amended): A system comprising:

a multi-frequency clock generator, wherein said multi-frequency clock generator outputs a first clock at a first frequency and a second clock at a second frequency;

a vertical scaler, wherein said vertical scaler receives said first clock at said first frequency from said multi-frequency clock generator, and wherein said vertical scaler receives a first plurality of video lines at said first frequency and outputs a second plurality of video lines at said first frequency;

a FIFO, wherein said FIFO receives said first clock at said first frequency and said second clock at said second frequency from said multi-frequency clock generator, and wherein said FIFO receives said second plurality of video lines at said first frequency from said vertical scaler, and wherein said FIFO outputs said second plurality of video lines at said second frequency such that said second plurality of video lines at said second frequency are horizontally scaled.

Claim 21 (original): The system of claim 20 wherein said second plurality of video lines are in a first video format.

Claim 22 (original): The system of claim 21 further comprising a modulator/timing generator, wherein said modulator/timing generator receives said second clock at said second frequency from said multi-frequency clock generator, wherein said modulator/timing generator receives said second plurality of video lines

from said FIFO in said first video format, and said modulator/timing generator converts said first video format into a second video format.

Claim 23 (original): The system of claim 22 wherein said first video format is selected from the group consisting of VGA and SVGA.

Claim 24 (original): The system of claim 22 wherein said second video format is selected from the group consisting of NTSC, PAL, SECAM, and SCART.

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Claim 25 (original): The system of claim 22 wherein said first video format is SVGA and said second video format is NTSC.

Claim 26 (original): The system of claim 20 wherein said first frequency is an integer ratio of said second frequency.

Claim 27 (original): The system of claim 20 wherein said first frequency is a non-integer ratio of said second frequency.

Claim 28 (original): The system of claim 20 wherein said first clock and said second clock are synchronous.

Claim 29 (original): The system of claim 20 wherein said first clock and said second clock are asynchronous.

Claim 30 (currently amended): A system comprising:

means for generating a first clock at a first frequency and a second clock at a second frequency;

means for scaling, wherein said means for scaling receives said first clock at said first frequency, and wherein said means for scaling receives a first plurality of video lines at said first frequency and outputs a second plurality of video lines at said first frequency;

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means for inputting and outputting, wherein said means for inputting and outputting receives said first clock at said first frequency and said second clock at said second frequency, and wherein said means for inputting and outputting receives said second plurality of video lines at said first frequency, and wherein said means for inputting and outputting outputs said second plurality of video lines at said second frequency such that said second plurality of video lines at said second frequency are horizontally scaled.

Claim 31 (previously presented): The system of claim 30 wherein said second plurality of video lines are in a first video format.

Claim 32 (previously presented): The system of claim 31 further comprising means for modulating, wherein said means for modulating receives said second clock at said second frequency and receives said second plurality of video lines in said first video format, wherein said means for modulating converts said first video format into a second video format.

Claim 33 (previously presented): The system of claim 32 wherein said first video format is selected from the group consisting of VGA and SVGA.

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Claim 34 (previously presented): The system of claim 32 wherein said second video format is selected from the group consisting of NTSC, PAL, SECAM, and SCART.

Claim 35 (previously presented): The system of claim 32 wherein said first video format is SVGA and said second video format is NTSC.

Claim 36 (previously presented): The system of claim 30 wherein said first frequency is an integer ratio of said second frequency.

Claim 37 (previously presented): The system of claim 30 wherein said first frequency is a non-integer ratio of said second frequency.

Claim 38 (previously presented): The system of claim 30 wherein said first clock and said second clock are synchronous.

cont.

Claim 39 (previously presented): The system of claim 30 wherein said first clock and said second clock are asynchronous.